SEMICONDUCTOR DEVICE

BACKGROUND

Conventionally, at least one STI (shallow trench insulator) is provided between a P doped region and an N doped region to separate the P doped region and the N doped region. FIG. **1** is a semiconductor device **100** with a STI **101** for related art. As shown in FIG. **1**, a STI **101** is provided between a P doped region **103** and an N doped region **105**. Therefore, a current path CP for transmitting currents from the P doped region **103** to the N doped region **105** must by-pass the STI **101** since materials of the STI **101** are not conductive. In such case, the current path CP is longer, such that the charge/discharge time for the semiconductor device is correspondingly extended, which may causes some disadvantages. For example, if the semiconductor device **100** is applied as an ESD device, the circuit protected by such device is easily broken since the semiconductor device **100** has a low discharge speed.

SUMMARY

Therefore, one objective of the present application is to provide a semiconductor device that can provide higher discharging speed.

In one embodiment, a semiconductor device comprising a substrate is disclosed. The substrate comprises: a well of type one; a first doped region of type two, provided in the well of type one; a well of type two, adjacent to the well of type one; and a first doped region of type one, doped in the well of type two. The substrate comprises no isolating material provided in a current path formed by the first doped region of type two, the well of type one, the well of type two and the first doped region of type one.

In some embodiments, the first type is N type and the second type is P type. In other embodiments, the first type is P type and the second type is N type.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a semiconductor device with a STI for related art.

FIG. **2** to FIG. **7** are top views and cross-sectional views for semiconductor devices, without silicide, according to embodiments of the present application.

FIG. **8** to FIG. **10** are cross-sectional views for semiconductor devices, with silicide, according to embodiments of the present application.

FIG. **11** is a circuit diagram illustrating a voltage providing circuit for providing voltages to the semiconductor devices disclosed in the present application, according to one embodiment of the present application.

DETAILED DESCRIPTION

FIG. **2** to FIG. **7** are top views and cross-sectional views for semiconductor devices according to embodiments of the present application. In the following embodiments, for the brevity of illustrating, a first type and a second type are applied to respectively indicate the N type or the P type. However, the first type and the second type indicate different meanings in different embodiments. In the embodiments of FIG. **2**, FIG. **4**, FIG. **6**, FIG. **8**(*a*), FIG. **9**(*a*), FIG. **10**(*a*), the first type indicates the N type, the second type indicates the P type. On the contrary, in the embodiments of FIG. **3**, FIG. **5**, FIG. **7**, FIG. **8**(*b*), FIG. **9**(*b*), FIG. **10**(*b*), the first type indicates the P type, the second type indicates the N type. Also, the following embodiment can be implemented by a SCR (Silicon Controlled Rectifier, but not limited.

Please refer to FIG. **2**, the semiconductor device **200** comprises a substrate S. The substrate S comprises: a well of type one W_**1**; a first doped region of type two D_**21**, provided in the well of type one W_**1**; a well of type two W_**2**, adjacent to the well of type one W_**1**; and a first doped region of type one D_**11**, doped in the well of type two W_**2**. The substrate S comprises no isolating material, such as above-mentioned STI, provided in a current path CP formed by the first doped region of type two D_**21**, the well of type one W_**1**, the well of type two W_**2** and the first doped region of type one D_**11**. In this embodiment, the current path CP is from IO to the VSS provided to the first doped region of type one D_**11**.

In the embodiment of FIG. **2**, the semiconductor device **200** further comprises a first conductive material CM_**1** and a second conductive CM_**2** (ex. poly silicide). The first conductive material CM_**1** is provided on the well of type one W_**1** and the well of type two W_**2** but not on the first doped region of type one D_**11** and the first doped region of type two D_**21**. Additionally, the second conductive layer CM_**2** is provided on the well of type two W_**2** but not on the first doped region of type one D_**11**. The first conductive material CM_**1** and the second conductive CM_**2** can receive different voltages TP, TN to assist the transmission of currents.

Moreover, the semiconductor device **200** can comprise a second doped region of type one D_**12** provided in the well of type two; and a second doped region of type two D_**22** provided in the well of type two W_**1**. The second doped region of type one D_**12** and the second doped region of type two D_**22** can assist the transmitting of currents. The second doped region of type two D_**22** and the second doped region of type one D_**12** are provided between the first doped region of type one D_**11** and the first doped region of type two D_**21**. In such case, the first conductive material CM_**1** is provided on a region between the first doped region of type two D_**21** and the second doped region of type two D_**22**. The second conductive material CM_**2** is provided on a region between the first doped region of type one D_**11** and the second doped region of type one D_**12**.

Please note during the process manufacturing the semiconductor device **200**, a protecting material P_**1** can be provided as shown in FIG. **2**. By this way, the silicide is not generated at the location of the protecting material P_**1**. Please refer to FIG. **8**(*a*), which illustrates an embodiments that the structure in FIG. **2** further comprises silicide SI. As shown in FIG. **8**(*a*), the silicide SI is not generated at the location of the protecting material P**1** shown in FIG. **2**. For more detail, in FIG. **8**(*a*) the silicide SI is not provided on at least part of the well of type one W_**1** adjacent to the first doped region of type two D_**21**, and at least part of the first doped region of type two D_**21** adjacent to the well of type one W_**1**.

Besides, the semiconductor device **200** in FIG. **2** can further comprise: a third doped region of type one D_**13**, doped in the well of type one W_**1**, not touching the first doped region of type two D_**21**; and a third doped region of type two D_**23**, doped in the well of type two W_**2**, touching the first doped region of type one D_**11**. The protecting